CLAIMS

1. A method of controlling the pixels of a liquid crystal display matrix which consists in briefly applying to a storage capacitor (Ca, Cb), associated with an elementary liquid crystal cell (LC), an analogue DC voltage (Vi) corresponding to a desired gray level, in linking a first terminal of the capacitor to the gate of a transistor (Ta, Tb) whose source is then linked to a ground and whose drain is linked to an electrode of the cell and is linked moreover to a voltage source Vdd across a current source (SC1), and in applying to a second terminal of the storage capacitor a DC voltage ramp varying monotonically for the duration of an image frame.

2. The method as claimed in claim 1, characterized in that the voltage ramp varies in an essentially linear manner between a zero voltage level and a voltage level substantially equal to the value of a switch-on threshold voltage VT of the transistor.

3. The method as claimed in claim 2, characterized in that the analogue DC voltage representing the gray level and applied to the storage capacitors varies between 0 volts and the same threshold voltage value VT.

4. The method as claimed in claim 3, characterized in that the liquid crystal cell receives a supply voltage Vdd for a fraction of a frame duration equal to Vi/VT or (VT-Vi)/VT and a zero voltage the remainder of the time.

5. The method as claimed in one of claims 1 to 4, characterized in that a ramp generator is associated with each row of the matrix, a ramp beginning after an analogue voltage has been charged into a storage capacitor of each of the dots of the row.

6. The method as claimed in one of claims 1 to 4, characterized in that two storage capacitors (Ca, Cb) and two transistors (Ta, Tb) are associated with each elementary liquid crystal cell, the first capacitor and the first transistor operating alternately with the second capacitor and the second transistor so as to store row by row an analogue voltage representing a gray level in the first capacitor during the even frames while the control of the cell is effected by the second transistor and the second capacitor, and so as to store row by row in the second capacitor an analogue voltage representing a gray level during the even frames while the control of the cell is effected by the first transistor and the second capacitor, the second terminal of the first storage capacitor being maintained at 0 volts during the odd frames and receiving a linear ramp during the even frames, and conversely the second terminal of the second capacitor being maintained at 0 volts during the even frames and receiving a linear ramp during the odd frames.

7. A liquid crystal matrix display, comprising an active matrix of image dots and peripheral circuits, the matrix comprising a cross array of addressing lines (L1a, L1b) and of columns (C1, C2) for feeding in analogue voltages representing the gray levels to be displayed on the dots of each row and, for each dot at the crossover of a row and of a column, an elementary electronic circuit for controlling an elementary liquid crystal cell situated at this crossover, the elementary circuit comprising:

- at least one storage capacitor (Ca, Cb) for storing for the duration of an image frame an analogue voltage (Vi) applied by the column, a first terminal of the storage capacitor being linked to the gate of the transistor (Ta, Tb),
- in series between two voltage supply terminals, an elementary current source (SC1) and a switching

transistor (Ta, Tb), the drain of the switching transistor being linked to the liquid crystal cell (LC),

the peripheral circuits comprising means for receiving a periodic voltage ramp (GR), common to all the cells of at least one row, the ramp being applied to a second terminal of the storage capacitor of the cells of this row.

8. The matrix display as claimed in claim 7, characterized in that the gate-source threshold voltage for switching on the transistor is VT, the ramp has an amplitude of VT, and the analogue voltage representing the gray level can vary between 0 and VT.

9. The matrix display as claimed in one of claims 7 and 8, characterized in that the elementary circuit associated with each image dot is a circuit with double memory comprising two storage capacitors (Ca, Cb) and two switching transistors linked to the same elementary cell (LC) and operating alternately one frame out of two, a voltage value being applied to a first capacitor (Ca) during an odd frame whereas the second capacitor (Cb) retains the voltage that it received during the previous even frame, and conversely, the circuit comprising a disabling facility (KT1a) for switching off the transistor linked to the first capacitor so as to disable the transistor during the odd frame and a disabling facility (KT1b) for switching off the transistor linked to the second capacitor so as to disable this transistor during the even frame.

10. The matrix display as claimed in claim 9, characterized in that it comprises means for applying a ramp to all the first capacitors during the even frames and for applying a ramp to all the second capacitors of the matrix during the odd frames.

11. The matrix display as claimed in one of Claims 7 and 8, characterized in that the elementary circuit associated with each image dot is a circuit with simple memory with a single storage capacitor and a single switching transistor, and in that means are provided for applying to the storage capacitors of a row of dots of the matrix a ramp which starts after an operation of storage in the capacitors of the cells of this row and which lasts for the remainder of a frame duration, the operations of storing analogue voltages in the capacitors being performed row by row.

12. The matrix display as claimed in one of claims 7 to 10, characterized in that it constitutes a color sequential display in which the consecutive image frames serve for the modulation of light of different colors.